REMARKS

Present Status of the Application

The Office Action mailed on February 22, 2002, rejected all claims 1-15. Specifically, the Office Action rejected claims 1-15 under 35 U.S.C. 112, second paragraph. The Office Action also objected to the specification. In addition, the Office Action rejected claims 1-15 under 35 U.S.C. 103, as being unpatentable over Applicant's Admitted Prior Art (AAPA, hereinafter) in view of Chester (U.S. Pat. No. 6,014,055). Applicants have amended the "summary of the invention" to overcome the objection to the specification. Applicants have also amended independent claims 1 and 8 above. Applicants respectfully submit that now new matter is added by way of these amendments. As amended, these claims clearly distinguish over Applicants' admitted prior art in view of Chester, and therefore overcome the rejections under 35 U.S.C. 103. After entry of the foregoing amendments, claims 1-15 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Summary of Applicant's Invention

The Applicant's invention is directed to a multi-level pulse width modulation (MPWM) digital-to-analog converter for receiving a n-bit pulse code modulation (PCM) signal and then outputting a m-level analog signal is provided. The MPWM DAC comprises a converter circuit, 2^m first output drivers, 2^m second output drivers and a control circuit. The converter circuit is used for converting (n-m) most significant bits (MSB) of the n-bit PWM signal into a PWM

waveform, and then generating a first input signal and a second input signal. Each of the 2^m first output drivers is used for receiving the first input signal, and then generating a first output current, wherein the first output currents of the 2^m first output drivers can be equal or not. Each of the 2^m second output drivers is used for receiving the second input signal, and then generating a second output current, wherein the second output currents of the 2^m first output drivers can be equal or not. The control circuit is coupled to the converter circuit, 2^m first output drivers, and 2^m second output drivers, for controlling the on-off status of each of the first and the second output drivers.

Discussion of Office Action Rejections

The specification is objected to because "SUMMARY OF THE INVENTION'' is not satisfied the requirement stated in MPEP 608.01(d). Applicants have amended "SUMMARY OF THE INVENTION" above to overcome the objection.

The Office Action rejected claims 1-15 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter. In response, Applicants have amended claim 1 above. In the amended claim 1, it clearly defines that the PCM signal has n bits, the total bits of the received PCM signal. Therefore, the numbers of n, m are well define and (n-m) bits in claim 1 becomes definite. In addition, each of m_1 and m_2, which are the numbers of the output drivers of the first and the second output driver devices respectively, is smaller than n. Namely, the number (m_1 or m_2) of output drivers is only defined to be smaller than the total bits (n) of the received PCM signal. Therefore, m_1 or m_2 are well defined. After

amended claim 1, Applicants respectfully submit that the rejection under 35 U.S.C 112 has been properly addressed and the rejection should be overcome.

Turning now to the substantive rejections, the Office Action rejected claims 1-15 under 35 U.S.C. 103(a), as being unpatentable over Admitted prior art (Fig.1, AAPA) in view of Chester. In response, Applicant respectfully traverses the rejection and the interpretations for at least reasons set forth as follows.

Applicants invention characterizes the requisite features recited in the independent claims 1 and 8, which are set forth immediately below:

> 1. (Once Amended) A multi-level pulse width modulation (MPWM) digital-to-analog converter for receiving a pulse code modulation (PCM) signal having n bits and then outputting a pulse width modulation (PWM) signal , comprising:
>
> a converter circuit for receiving the PCM signal to convert (n-m) bits of the PCM signal into the PWM signal, wherein m is the number of the least significant bit (LSB) signal of the PCM signal and n>m, and then generating a first input signal, a second input signal and an enabling signal;
>
> a control device for receiving the enabling signal to generate a control signal;
>
> a first output driver device having 2^{m1} output drivers (m_1<n) for receiving the first input signal and the control signal, and then outputting a first driving signal, ***wherein sum of output currents of the 2^{m1} output drivers is equal to a maximum output current of the first output driver device***;
>
> a second output driver device having 2^{m2} output drivers (m_2<n) for receiving the second input signal and the control signal, and then outputting a second driving signal, ***wherein sum of output currents of the 2^{m2} output drivers is equal to a maximum output current of the second output driver device; and***
>
> ***an output device for receiving the first and the second driving signals and then outputting the PWM signal***;
>
> wherein in response to the least significant bit (LSB) signal of the PCM signal, the control device selects and disables ***in a specified interval of each***

> ***sampling cycle such that the output drivers the first and the second output driver devices are in a high impedance status, to control outputs of the first and the second output driver devices.***

(*Emphasis added*). Also, claim 8 recites requisite features as follows.

> 8. (Once Amended) A multi-level pulse width modulation (MPWM) digital-to-analog converter for receiving a digital signal, wherein the digital signal comprises at least one modulated bit and at least one level bit and then outputs an analog modulated signal, comprising:
>
> a converter circuit for receiving the digital signal and then converting the modulated bit into a first output signal, a second output signal, and the converter circuit outputting the first output signal, the second output signal and the level bit of the digital signal;
>
> a control device for receiving the level bit of the digital signal to generate a control signal;
>
> a plurality of first output drivers for receiving the first input signal and the control signal, and then outputting a first driving signal, ***wherein sum of output currents of the first output drivers is equal to a maximum output current corresponding to the first driving signal***;
>
> a plurality of second output drivers for receiving the second input signal and the control signal, and then outputting a second driving signal, ***wherein sum of output currents of the first output drivers is equal to a maximum output current corresponding to the first driving signal;*** and
>
> an output device for receiving the first and the second driving signals and then outputting the analog modulated signal.

(*Emphasis added*). Applicant respectfully submits that independent claims 1 and 8 patently define over the prior art for at least the reason that the prior art fails to adequately disclose those features emphasized above.

Clams 1-15 were rejected under 35 U.S.C. 102(a) as being unpatentable over AAPA in view of Chester. The Office Acton alleged that the AAPA discloses a multilevel pulse width modulation D/A converter, but fails to teach a control device that selects and disables the output

drivers in response to the control signal. The Office Action stated that lacked portion is disclosed by Chester, and one skilled in this art can combine the teachings of Chester to the AAPA. Therefore, the Office Action rendered that the present invention is unpatentable over AAPA in view of Chester. In response, Applicants respectfully traverse the rejection and the interpretations for at least reasons provided below.

First, Chester discloses a converter capable of converting different types of PCM signals to PWM signals. Namely, Chester's converter can convert various PCM types to the PWM signals. According to the Abstract, the PCM signal can be a symmetric PCM, a trailing edge PCM, and a leading edge PCM (*also, col. 2, lines 60-65*).

In addition, according to Chester's disclosure, when receiving a PCM input, its sign bit (the first bit) is stripped off. The remained N-1 bits of the PCM are divided into K bits (MSB) and L bits (LSB). The PCM signal can be converted to a PWM signal according to a sawtooth wave from a sawtooth wave generator 42 (see Fig. 4), the LSB and the MSB. The detail process can refer to Chester's col. 4, lines 35-67 and col. 5. When the pulse output is off, the amplifier will output 0 volts, and when the pulse output is on, the amplifier will output -V volts. Therefore, according to Chester's teachings, the output of the amplifier is either 0 or –V, and the pulse output must be on or off, which means that the PWM output is only a two-level signal (*col. 5, lines 26-42*). As discussed above, Chester fails to disclose, teach or suggest a method or a device that the PCM input can be converted to a multi-level PWM output.

In contrast, according to the invention, the present invention provides a solution capable of outputting multilevel PWM (greater than two levels) so that the PCM values can be represented by fractional values like X, X+1/4, X+2/4, and X+3/4, etc. In the invention, each of the first and the second output driver devices has a number of output drivers (buffers). The sum of the output currents (driving currents) of the output drivers is equal to the maximum out put current of the first (second) output driver. The output current of the output driver becomes fractional with respect to the maximum out put current of the first (second) output driver, which means that a multilevel PWM output can be provided. These requisite features are not disclosed, taught or suggested by Chester.

For at least the above reasons, the features claimed in the present invention are clearly different from the Chester's teachings.

In addition, the Office Action alleged the AAPA is a multilevel PWM D/A converter. However, Applicants want to provide a solution capable of converting a PCM input to a multilevel PWM output. Applicants clearly describe ***the prior art technology only provides a PWM D/A converter that can only provide two-level PWM (only 0 or 1)***. Referring to Fig. 1 of the invention, the output PWM waveforms of the first and the second output drivers 22, 24 contains only two logic levels of "0" and "1". Therefore, ***the AAPA is not a multilevel PWM D/A converter as alleged by the examiner.***

As described above, because Chester's converter cannot provide a multilevel PWM output and the AAPA is not a multilevel PWM D/A converter, the cited combination still provide

a converter having a two-level PWM output. In the other word, either Chester or AAPA cannot provide fractional PWM output, like X, X+1/4, X+2/4 and X+3/4 as disclosed in the invention.

For at least the reasons set out above, either Chester or AAPA fails to teaches multilevel PWM outputs or fractional outputs, and the cited combination also fails to teaches multilevel PWM outputs or fractional outputs. In addition, Chester also fails to teach that output driver device comprises a number of output buffers or drivers (smaller than the total bits of the PCM input), in which the sum of the current outputs of the output drivers (buffers) is equal to a maximum output current of the output drive (*refer to amended claim 1 of the invention*). Therefore, the invention clearly distinguishes over the AAPA in view of Chester.

For at least the foregoing reasons, Applicants respectfully submit that independent claims 1 and 8 patently define over the prior art, and should be allowed. For at least the same reasons, dependent claims 2-7 and 9-15 patently define over the prior art as well.

CONCLUSION

For at least the foregoing reasons, it is believe that all pending claims 1-15 are in proper condition for allowance. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is hereby invited to telephone the undersigned counsel to arrange for such a conference.

Atty Docket No.: JCLA6047 **Serial No.: 09/750,819**

Respectfully submitted,
J.C. PATENTS

Date: 5/3/2002

Jiawei Huang
Registration No. 43,330

4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax: (949)-660-0809

Atty Docket No.: JCLA6047 Serial No.: 09/750,819

ANNOTATED VERSION OF MODIFIED CLAIMS TO SHOW CHANGES MADE

In The Specification

Please amend the "SUMMARY OF THE INVENTION" as follows

As embodied and broadly described herein, the invention provides a multi-level pulse width modulation (MPWM) digital-to-analog converter (DAC) for receiving a pulse code modulation (PCM) signal having n bits and then outputting a pulse width modulation (PWM) signal. The MPWM DAC comprises a converter circuit, a control device, a first output driver device, a second output driver device and an output device.

The converter circuit [is used for receiving n-bits of the PCM signal to converter] converts [the] (n-m) bits of the PCM signal into the PWM signal, wherein m is the number of the least significant bit (LSB) signal of the PCM signal and n>m. [And then the converter circuit generates a first input signal, a second input signal and an enabling signal. The control device receives the enabling signal to generate a control signal. The] Each of the first output driver device and the second output driver has different number of output drivers, thereby the output PWM signal is a multi-level signal, rather that a two-level signal in the prior art. [has 2^{m1} output drivers (m1<n) for receiving the first input signal and the control signal, and then outputting a first driving signal, while the second output driver device has 2^{m2} output drivers (m2<n) for receiving the second input signal and the control signal, and then outputting a second driving

signal. The output device can receive the first and the second driving signals and then output the PWM signal.]

[In response to the least significant bit (LSB) signal of the PCM signal, the control device selects and disables in a specified interval of each sampling cycle such that the output drivers the first and the second output driver devices are in a high impedance status, by which the control device is capable of controlling outputs of the first and the second output driver devices.]

[Accordingly the output current of each output driver is a fraction of the output current of the output driver of the conventional PWM DAC, and therefore, the minimum output unit of the MPWM DAC of the present invention is fractional, such as 1/4. The PCM values, such as X+(1/4), X+(2/4) and X+(3/4), etc., can be easily represented. Advantageously, using the MPWM DAC of the present invention not only increases the resolution, but also remain the sampling rate.]

In The Claims

Please amend independent claims 1 and 8 as follows

1. (Once Amended) A multi-level pulse width modulation (MPWM) digital-to-analog converter for receiving a pulse code modulation (PCM) signal having n bits and then outputting a pulse width modulation (PWM) signal , comprising:

a converter circuit for receiving [n-bits of] the PCM signal to [converter] convert [the] (n-m) bits of the PCM signal into the PWM signal, wherein m is the number of the least significant

bit (LSB) signal of the PCM signal and n>m, and then generating a first input signal, a second input signal and an enabling signal;

a control device for receiving the enabling signal to generate a control signal;

a first output driver device having 2^{m1} output drivers (m1<n) for receiving the first input signal and the control signal, and then outputting a first driving signal, wherein sum of output currents of the 2^{m1} output drivers is equal to a maximum output current of the first output driver device;

a second output driver device having 2^{m2} output drivers (m2<n) for receiving the second input signal and the control signal, and then outputting a second driving signal, wherein sum of output currents of the 2^{m2} output drivers is equal to a maximum output current of the second output driver device; and

an output device for receiving the first and the second driving signals and then outputting the PWM signal;

wherein in response to the least significant bit (LSB) signal of the PCM signal, the control device selects and disables in a specified interval of each sampling cycle such that the output drivers the first and the second output driver devices are in a high impedance status, to control outputs of the first and the second output driver devices.

8. (Once Amended) A multi-level pulse width modulation (MPWM) digital-to-analog converter for receiving a digital signal, wherein the digital signal comprises at least one modulated bit and at least one level bit and then outputs an analog modulated signal, comprising:

a converter circuit for receiving the digital signal and then converting the modulated bit into a first output signal, a second output signal, and the converter circuit outputting the first output signal, the second output signal and the level bit of the digital signal;

a control device for receiving the level bit of the digital signal to generate a control signal;

a plurality of first output drivers for receiving the first input signal and the control signal, and then outputting a first driving signal, wherein sum of output currents of the first output drivers is equal to a maximum output current corresponding to the first driving signal;

a plurality of second output drivers for receiving the second input signal and the control signal, and then outputting a second driving signal, wherein sum of output currents of the first output drivers is equal to a maximum output current corresponding to the first driving signal; and

an output device for receiving the first and the second driving signals and then outputting the analog modulated signal.